METHOD AND APPARATUS FOR FACILITATING RANDOM PATTERN TESTING OF LOGIC STRUCTURES

ABSTRACT

[0034] A method for preparing a logic structure for random pattern testing is disclosed. In an exemplary embodiment of the invention, the method includes configuring a select mechanism within a data scan chain, the select mechanism configured between a first register in the data scan chain and a second register. A parallel data path is routed within the scan chain, the parallel data path beginning from an input side of the first register, running through the select mechanism, and ending at an input side of the second register. Thus configured, the select mechanism is capable of switching a source path of input data to said second register from a normal data path to the parallel data path. When the parallel data path is selected as the source path of input data to the second register, data loaded into the second register matches data loaded into the first register.